**DIRECTORATE OF TECHNICAL EDUCATION**

**DIPLOMA IN ELECTRONICS AND COMMUNICATION ENGINEERING**

**III YEAR**

**M SCHEME**

**VI SEMESTER**

**2015-2016 onwards**

# TEST ENGINEERING

**CURRICULAM DEVELOPMENT CENTRE**

**M-SCHEME**

**(Implemented from the Academic year 2015-2016 onwards)**

**Course Name: Electronics and Communication Engineering**

**Subject code : 34062**

**Semester : VI Semester**

**Subject title : TEST ENGINEERING**

## TEACHING AND SCHEME OF EXAMINATION:

Number of Weeks/ Semester : 15 weeks

| Subject | Instruction | | Examination | | | |
|---|---|---|---|---|---|---|
| Test Engineering | Hrs/ week | Hrs/ semester | Marks | | | Duration |
| | | | INTERNAL ASSESMENT | BOARD EXAM | TOTAL | |
| | 6 | 90 | 25 | 75 | 100 | 3Hrs |

## TOPICS AND ALLOCATION:

| Unit | TOPIC | Hrs |
|---|---|---|
| I | INTRODUCTION TO TEST ENGINEERING | 17 |
| II | AUTOMATED TESTING METHODS AND TECHNOLOGY | 17 |
| III | V-I(SIGNATURE) TESTING METHODS AND TECHNOLOGY | 15 |
| IV | BOUNDARY SCAN TESTING METHODS AND TECHNOLOGY | 15 |
| V | ATE TEST PROGRAM GENERATION AND SEMICONDUCTOR TESTING | 16 |
| | Revision & Test | 10 |
| | TOTAL | 90 |

## 34062 - TEST ENGINEERING

### DETAILED SYLLABUS

| UNIT | NAME OF THE TOPIC | HOURS |
|---|---|---|
| 1 | **INTRODUCTION TO TEST ENGINEERING.**<br><br>Need and Importance of Test Engineering – Principles of Fundamental Testing Methods – Basic Principles of Memory Testing – PCB Track Short Testing Methods –Concepts of Trouble Shooting PCBs - Manual and Automated PCB Trouble Shooting Techniques. | **17** |
| 2 | **AUTOMATED TESTING METHODS AND TECHNOLOGY**<br><br>Introduction to Automated Test Techniques – Fundamental of Digital Logic Families - Concepts of Back-Driving / Node Forcing Technique and its International Defense Standard - Concepts of Digital Guarding - Auto Compensation - Clock Termination – Functional Test Methods - Functional Testing of Digital, Analog and Mixed Integrated Circuit – Different types of Memory Module Functional Test. | **17** |
| 3 | **V-I(Signature) TESTING METHODS AND TECHNOLOGY**<br><br>Fundamentals of Electrical Characteristics - Effects of Curve Trace, Characteristics of Passive and Active Components - Understanding Composite VI-Curve and it deviations – Component Identification of Ageing Effects with VI Curve Trace, Input and Output Characteristics of Digital Integrated Circuits - Good Versus Suspect interpretation Comparison. | **15** |
| 4 | **BOUNDARY SCAN TESTING METHODS AND TECHNOLOGY**<br><br>Introduction to Boundary Scan – Need of Boundary Scan Test Technique - Principle of Boundary Scan Test - Boundary Scan Architecture - Application of Boundary Scan Test- Boundary Scan Standards - Boundary Scan Description Language (BSDL) – Interconnect test – Serial Vector Format (SVF) Test - Basic of JTAG Port - Digital Integrated Circuit Test using Boundary Scan Techniques. | **15** |
| 5 | **ATE Test Program generation And Semiconductor testing**<br><br>ATE in PCB Test – Test Fixtures - Basics of Automatic Test Program Generation - Standard Test Data Format STDF – Basic of Digital Simulator - Introduction to Semiconductor Test, Use of Load Boards. | **16** |

**REFERENCE BOOKS**:


1. Test Engineering for Electronic Hardware – S R Sabapathi, Qmax Test Equipments P Ltd., 2011.

2. Practical El**e**ctronic Fault Finding and Trouble shooting by Robin Pain Newnes, Reed Educational and professional publishing Ltd., 1996
3. The Fundamentals of Digital Semiconductor Testing, Floyd, Pearson Education India, Sep-2005